A Detailed Model for a Thyristor Based Static Transfer Switch

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Abstract—Industrial customers often suffer from supply voltage interruptions and sags due to the increase in the utilization of sensitive equipment in the process automation and control. An effective way to improve power quality and reliability of sensitive customers is to use a Static Transfer Switch. This device enables a very fast change in the supply of the customer to an alternate feeder providing adequate power conditioning for several power quality problems, such as voltage sags, swells and interruptions. In this paper, an analytical model of STS is proposed and its performance is verified using the ElectroMagnetic Transients for DC(EMTDC) simulation package. Simulations using this model are performed in order to handle voltage sags based on real measurements on an actual industrial customer’s supply voltage. Different phase angles and magnitudes of the two alternate source pre-fault voltages and different fault instances are considered.

Index Terms—Bus transfer, power conditioning, power quality, power system simulation, sensitive loads, static transfer switch, voltage sags.

I. INTRODUCTION

The increasing sensitivity of consumer equipment, have given rise to growing interest concerning the “quality” of the electric power. Voltage sags of even low magnitude and short duration can cause financial losses to industrial customers due to process down-time, lost production, idle work forces and other factors[1]. There is a growing need, therefore, for power conditioning devices that will act very fast resulting in mild voltage sags of minimum duration experienced by the load. Many devices based on Power Electronics Technology have been proposed and applied in many cases where mitigation of voltage sags is needed. The Static Transfer Switch(STS), the Dynamic Voltage Restorer(DVR), the Distribution Static Compensator(DSTATCOM), the Static Var Compensator(SVC) and the Solid State Tap Changer(SSTC) are the most used devices.

One of the most effective solutions from the aforementioned is the Static Transfer Switch(STS). If an alternate feeder exists or can be provided to the critical load at reasonable cost, STS can transfer quickly enough the voltage supply to an alternate source and sensitive load experiences only a shallow sag of short duration. Obviously, STS is not effective in the event of a utility complete outage and cannot provide power conditioning, if both feeders sag in voltage simultaneously, as might be the case for a fault near the point where the two feeders join[2].

The voltage sag magnitude(VSM) and duration(VSD) at the load terminals, depend directly on the STS control scheme. Hence, voltage detection and transfer need to be as fast as possible. Furthermore, transfer and gating logic must assure that in no case paralleling of the sources will occur, which would cause severe damage to thyristor switches. Detection and transfer schemes have already been proposed and experimentally tested[4] under the assumption of almost zero difference in phase angle and magnitude between preferred and alternate source pre-fault voltages. The effect of fault type and severity, the effect of regenerative loads on the transfer time(TT), and the maximum transfer time, have also been discussed[5]-[7], under the same assumptions.

In actual practice, however, two feeders can have a quite large difference in voltage phase angles and a small difference in magnitudes. In this paper, a voltage detection method and a transfer strategy are proposed taking into account these differences. STS performance at the terminals of an actual industrial customer in Greece suffering from voltage sags, is evaluated by simulations in EMTDC[11]. Real measurements at the load supply voltage terminals are used to verify the performance of the STS model. In every case studied, minimum, maximum and average values of detection time(DT), TT, VSM and VSD, are calculated.

II. STS STRUCTURE

A. Power circuit of the STS

The three-phase model of a STS is shown in Figure 1. It consists of two thyristor blocks at the P(referred) and A(lternate) source, which connect the load to the two alternate sources. Each thyristor block is composed of three thyristor modules corresponding to the three phases of the system. In each thyristor module, two sets of thyristor switches are connected in opposite directions, e.g. PP1/PN1 and AP1/AN1, to allow the load current to flow in both positive and negative directions. Mechanical bypass switches Pb and Ab are used in parallel with the thyristor blocks A and P, respectively to supply the load, even if the thyristor switches are out of operation. Isolator switches M1p / M1a and M2p / M2a are also used to isolate the thyristor blocks from the rest of the
system for maintenance of thyristor modules and test purposes[4].

**B. Control circuit of the STS**

The control circuit of the proposed STS is shown in Figure 2. It consists of two parts: the voltage detection circuit and the commutation-gating circuit. The control circuit takes as input the voltage magnitudes of the two feeders and performs a load-transfer when needed. When a deviation from the pre-set limits on the preferred source is detected, a transfer signal is generated. Index 1 shows that transfer to the alternate source is effected, while index 0 shows transfer to the preferred source. When the conditions for a safe commutation at each phase separately are fulfilled, load is completely transferred to the alternate source, until the voltage on the preferred source is restored. For the transfer to the preferred source, current zero-crossing is only detected. The outputs of the control circuit are the pulses for the preferred and alternate source thyristor switches[4].

![Fig. 1. Static transfer switch](image1)

**Commutation and Gating Circuits**

![Fig. 2. Control circuit configuration of the STS](image2)

**B1. Voltage detection strategy**

The proposed voltage detection circuit is presented in Figure 3. It is very simple and easy to implement and has been proved to be very accurate and fast, even in the case of a shallow sag.

The instant phase voltages are digitally sampled (sampling frequency=10 kHz) and the rms value is calculated by squaring and integrating the produced signal using the circuit shown in Figure 3a. A second order transfer functions is used to enable a fast response of the calculated rms voltage to any voltage fluctuations, as shown in Figure 3b. By taking the minimum of the three rms phase voltages, the response becomes even faster. Next, the deviation from the preset reference voltage (e.g. 1.0 pu) is compared to a tolerance limit (here it has been set to 10%[11]). When the voltage on the preferred source is within tolerance, control logic turns on the corresponding thyristors. Power then can flow from the preferred source to the load. If voltage deviates from the tolerance limit, the control logic checks the voltage of the alternate source, otherwise, it does not issue any changes in the feeding source of the load. When the voltage on the preferred source returns to acceptable values, load is transferred back to the preferred source after a time delay (a few cycles are enough) to ensure that preferred source phase voltages are perfectly restored.

![Fig. 3a. Rms meter](image3)

![Fig. 3b. Voltage detection circuit configuration](image4)
B.2 Commutation and gating strategy

A fast and safe commutation of the preferred source thyristor switches for every phase, depends directly on the relative position and magnitude of three variables when a voltage sag is detected:

1. Preferred source instant phase voltage (e.g. \( V_{a_p}(t) \))
2. Alternate source instant phase voltage (e.g. \( V_{a_a}(t) \))
3. Preferred source instant line current (e.g. \( I_{a_p}(t) \))

Subsequently, transfer time is directly related to the following parameters:

- The phase angle difference between the pre-fault phase voltages of the two alternate sources. This may be between 0 and 40° depending on the line impedance and the active and reactive power transferred to the load.
- The pre-fault voltage magnitude of the alternate source.
- The load power factor, which determines the position of the current with respect to the voltage on the preferred source[7].
- The severity of the fault which determines the value of the instant voltage on the preferred source when a transfer signal is initiated[7].
- The phase angle jump the fault introduces.
- The post-fault phase voltages, thus the type of the fault[7].
- The instant at which the fault occurs[7].

Hence, the commutation from one source to another requires some critical conditions to be fulfilled(Figure 2), in order to enable fast transferring to alternate source and to avoid false switching off of thyristor switches. This would lead to a cross current flowing through an outgoing(incoming) thyristor of one phase of the alternate source and through an incoming(outgoing) thyristor of a corresponding phase of the preferred source, which will feed the fault current[6]. Furthermore, turn-off time of thyristor switches is not constant but depends on manufacturer’s specifications, voltage level, natural conditions(e.g. temperature), reapplied dv/dt, reapplied di/dt and gate bias during the turn-off interval[8]. This means that a reverse voltage must be kept for a certain amount of time in order to assure successful commutation of thyristor switches.

Therefore, a transfer strategy which will take into account the relative position and magnitude of corresponding instant phase voltages of the two alternate sources and corresponding instant line current on the preferred source, is needed. Transferring does not always occur simultaneously for every phase. Each phase has to wait for one of the following conditions to become true in order to initiate transferring:

I. A) The three aforementioned variables are of the same sign and
B) The instantaneous difference in absolute voltage magnitude(e.g. \(|V_{a_p}(t)| - |V_{a_a}(t)|\)) is larger than a certain limit \( \Delta V_{1\text{min}} \), in order to give thyristor switch, which conducts at that moment, enough time to turn off. An example where condition A initiates transferring on phase - a is depicted in Figure 4a. Fault occurs at \( t=0.028 \) s, transfer signal is generated(voltage sag is detected) at \( t=0.032 \) s and transferring(only for phase - a) is initiated at \( t=0.0325 \) s. Thyristor PP1 is forced to turn off by turning on thyristor AP1(figure 1). It can be seen that Debloack Signal (dblk_altsrc_a), which enables firing pulses of alternate phase –a thyristor switches, is delayed for a short time in order to assure that voltage difference is within the preset limit. Furthermore, as expected, the two instant phase voltages become equal when alternate source phase –a thyristor AP1 is fired, until thyristor PP1 is completely turned-off. In this particular case, a smaller difference in instantaneous voltages ( \( |V_{a_p}(t)| - |V_{a_a}(t)| \) ) might have been able to lead to a safe commutation of thyristor switch. However, in a different case (Figure 4b), this smaller difference would lead to a high cross current because thyristor switch PP1 would not have enough time to turn off. Fault occurs at \( t=0.028 \) s and transfer signal as well as transferring are initiated at \( t=0.0295 \) s. Thyristor PP1 is forced to turn off by turning on thyristor AP1(figure 1), but given time is not enough. Eventually, PP1 does not turn off and when AN1 is turned on, a large current(about 3 times larger than in normal operation) flows from the alternate source through AN1 and PP1 feeding the fault located upwards the load on the preferred source. Hence, a certain value in voltage difference needs to be applied in every case to assure safe transferring.

II. A) If condition I-A is true but I-B is not, transfer logic delays until line current(e.g. \( I_{a_p}(t) \)) crosses zero, and
B) If \( (|V_{a_p}(t)| - |V_{a_a}(t)|) > 0 \) applies, initiates transferring (Figure 5). Fault occurs at \( t=0.022 \) s, transfer signal is generated at \( t=0.0277 \) s and transferring is initiated at \( t=0.0296 \) s.

III.A) If II_B does not apply when line current(e.g. \( I_{a_p}(t) \)) crosses zero but the three variables are of the same sign transferring is issued when:
B) \( (|V_{a_p}(t)| - |V_{a_a}(t)|) > 0 \) for the first time(Figure 6). Fault occurs at \( t=0.032 \) s, transfer signal is generated at \( t=0.0337 \) s and transferring is initiated at \( t=0.0372 \) s.

IV.A) Another important case is the one shown in Figure 7. \( V_{a_a}(t) \) and \( I_{a_p}(t) \) are of the same sign and \( V_{a_p}(t) \) of opposite sign, when a transfer signal is issued. In this case transferring can be initiated to reduce transfer time, when:
B) \( |V_{a_p}(t)| - |V_{a_a}(t)| > \Delta V_{2\text{min}} \) to assure successful commutation of thyristor PP1. Fault occurs at \( t=0.027 \) s detected at \( t=0.0293 \) s. At that time, \( V_{a_p}(t) \) takes values of opposite sign with respect to \( V_{a_a}(t) \) and \( I_{a_p}(t) \) values. Furthermore, \( |V_{a_p}(t)| - |V_{a_a}(t)| \) is larger than the preset value \( \Delta V_{2\text{min}} \), so transferring can be initiated. Obviously, if transferring was not issued at the time shown in Figure 7, it could be done to satisfy condition
III approximately 3 ms later, as shown by the intersection of the voltage waveforms at t=0.032 s.

Fig. 4a. Instant phase voltages and line currents of phase –a (for both alternate sources), where condition I initiates transferring.

Fig. 4b. Instant phase voltages and line currents of phase -a where commutation fails.

Fig. 5. Instant phase voltages and line currents of phase -a for a voltage sag where condition II initiates transferring.

Fig. 6. Instant phase voltages and line currents of phase -a for a voltage sag where condition III initiates transferring.

Fig. 7. Instant phase voltages and line currents of phase –a for a voltage sag where condition IV initiates transferring.

When voltage on the preferred source returns to its acceptable limits, another transfer is needed. To ensure that all three phase voltages are completely restored, a short delay of 80 ms was introduced. When the transfer signal finally becomes zero, all thyristors of alternate source side of the STS are switched off immediately and thyristors of preferred source side are switched on at the first zero current.

III. STUDY CASE

A. Power system configuration and measured events

To evaluate the performance of the proposed STS, an actual case of a sensitive load (a papermill) was studied. The installation of this consumer contains protection systems that trip immediately after even shallow sags with only a short duration. To investigate the frequency and characteristics of voltage sags experienced by this load, measurements of voltage sags were taken at the load terminals. These measurements are used to validate in a more realistic way the proposed model of the STS. Three characteristic sags are presented in Table I.
A simplified single-phase diagram of the equivalent network is shown in Figure 8. The critical load is fed by a 150/20 kV substation. Fault is arbitrarily applied on the 150 kV side and it is implemented using four switches to short-circuit the three phases. The duration, in which every fault switch is on, varies in order to obtain different sag duration per phase. Furthermore, different values of resistors and inductors are connected between phases to obtain different sag magnitude for each phase.

### B. Simulation results of the measured events

Voltage sag measurements shown in Table 1 were simulated using EMTDC. The results are shown in Figures 9a, 9b, and 9c.

<table>
<thead>
<tr>
<th>Event</th>
<th>Sag Duration (ms)</th>
<th>Phase -a Sag Magnitude (%)</th>
<th>Phase -b Sag Magnitude (%)</th>
<th>Phase -c Sag Magnitude (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>360</td>
<td>63.2</td>
<td>65.5</td>
<td>62.3</td>
</tr>
<tr>
<td></td>
<td>400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>170</td>
<td>75.0</td>
<td>78.0</td>
<td>71.0</td>
</tr>
<tr>
<td></td>
<td>180</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>40</td>
<td>77.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>82.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### TABLE I
VOLTAGE SAG MEASUREMENTS AT THE LOAD TERMINALS (SAG MAGNITUDE : THE REMAINING VOLTAGE MAGNITUDE).

#### C. STS performance

In the following simulations, $\Delta V_{1\text{min}}$ (condition I-B) and $\Delta V_{2\text{min}}$ (condition IV-B) are set to 0.6 pu and 0.35 pu (Base phase voltage equals 11.54 kV), respectively. These values ensure that no commutation failure occurs, as shown by a large number of simulations. STS performance on each event taking arbitrary initial conditions, is described below:

- **Event 1**
  The simulation results regarding the behaviour of the proposed model on the event 1, are depicted in Figures 10a, b, and c. The event occurred at $t_{\text{fault}} = 13 \text{ ms}$, detected at $t_{\text{det}} = 14.6 \text{ ms}$ and transfer was completed at $t_{\text{transf}} = 24.2 \text{ ms}$. The resulting sag magnitude was 71.13% and its duration was 18.78 ms. It must be noted that voltage on the alternate feeder was set to lead voltage on the preferred feeder by 20° just before the event occurred, and their magnitudes were: $V_{p\text{bef}} = 1.0 \text{ pu}$ and $V_{a\text{bef}} = 0.95 \text{ pu}$.

- **Event 2**

- **Event 3**

#### Fig. 9a. Simulation results of the rms phase voltages at the load terminals (Event 1).
#### Fig. 9b. Simulation results of the rms phase voltages at the load terminals (Event 2).
#### Fig. 9c. Simulation results of the rms phase voltages at the load terminals (Event 3).
#### Fig. 10a. Rms voltages with and without STS (Event 1).
As it can be seen in Figure 10b, it was condition III that was fulfilled and led to successful commutation in all three phases. It is the nature of the fault and the phase angle jump it leads to, together with the angle difference between the two feeders’ voltage, that makes condition III to be the most likely condition to initiate commutation, no matter what are the voltage magnitudes of the two feeders just before the fault and the time at which fault occurred.

**Event 2**

The simulation results for the event 2, are shown on Figures 11a, b, and c. The event occurred at $t_{\text{fault}} = 20 \text{ ms}$, detected at $t_{\text{det}} = 22.8 \text{ ms}$ and transfer was completed at $t_{\text{transf}} = 24 \text{ ms}$. The resulting sag magnitude was 71.52% and its duration was 12.06 ms. Voltage on the alternate feeder was set to lag the voltage on the preferred feeder by 40° just before the event occurred, and their magnitudes were: $V_{\text{p}}^{\text{bef}} = 1.0 \text{ pu}$ and $V_{\text{a}}^{\text{bef}} = 1.0 \text{ pu}$.

**Event 3**

The simulation results for the event 3, are presented on Figures 12a, b, and c. The event occurred at $t_{\text{fault}} = 12 \text{ ms}$, detected at $t_{\text{det}} = 13.96 \text{ ms}$ and transfer was completed at $t_{\text{transf}} = 23.26 \text{ ms}$. The resulting sag magnitude was 83.73% and its duration was 10.48 ms. Voltage on the alternate feeder was set to lag the voltage on the preferred feeder by 20° just before the event occurred, and their magnitudes were: $V_{\text{p}}^{\text{bef}} = 1.0 \text{ pu}$ and $V_{\text{a}}^{\text{bef}} = 1.0 \text{ pu}$.
Values (load power factor is considered constant and equal to 0.9) are:

1. **Instant at which fault occurred.** The half-period of instant voltage (preference source phase – an instant voltage was used as a reference) was divided into 20 equal intervals of 0.5 ms (9 degrees), at which the fault was applied.

2. **Pre-fault rms voltage on the alternate feeder \( V_{f_a} \).** Voltage magnitude on preferred source was set to 1.0 pu for all runs and voltage magnitude on alternate source was 1.0 or 0.95 pu.

3. **Phase angle difference in the two sources voltage.** \( \Phi_p \) was set to 0° and \( \Phi_a \) was set to take a value between –40° and 40° with a step of 10°.

Results based on all the combinations of the above parameters (378 runs per event) are presented in Table II. The minimum, maximum and average values are shown. Transfer Time is the time between the detection time and complete transferring (all three phases of the preferred source have turned off and all phases of alternate source have turned on) while Total-load Transfer Time (TLTT) represents the sum of the Detection Time and Transfer Time. To assure that commutation did not fail in any of those runs, maximum value of the three instant line currents of preferred source is measured for every run. A comparison between results in Table II and voltage tolerance limits of various industrial equipment shown in Table III[10], clearly shows that problems should not be anticipated by the sag magnitude and duration experienced by the load, when this STS is used. It should be noted here that detection time is expected to be a few µs longer in a real system, so VSM and VSD are expected to be a bit lower and longer respectively.

### TABLE II

**SUMMARIZATION OF RESULTS BASED ON 378 RUNS PER EVENT**

<table>
<thead>
<tr>
<th>Event</th>
<th>Min</th>
<th>Max</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sag Magnitude (%)</td>
<td>Sag Duration (ms)</td>
<td>Detection Time (ms)</td>
<td>Transfer Time (ms)</td>
</tr>
<tr>
<td>1</td>
<td>66.3</td>
<td>3.8</td>
<td>1.1</td>
</tr>
<tr>
<td>2</td>
<td>86.8</td>
<td>18.3</td>
<td>1.7</td>
</tr>
<tr>
<td>3</td>
<td>75.5</td>
<td>13.2</td>
<td>1.3</td>
</tr>
</tbody>
</table>

### TABLE III

**VOLTAGE TOLERANCE LIMITS OF VARIOUS EQUIPMENT PRESENTLY IN USE ACCORDING TO IEEE STD. 1346.**

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Voltage Tolerance (On Average)*</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLC</td>
<td>260 ms , 60 %</td>
</tr>
<tr>
<td>PLC input card</td>
<td>50 ms , 35 %</td>
</tr>
<tr>
<td>5 kVA ac drive</td>
<td>50 ms , 75 %</td>
</tr>
<tr>
<td>Ac control relay</td>
<td>20 ms , 65 %</td>
</tr>
<tr>
<td>Motor starter</td>
<td>50 ms , 50 %</td>
</tr>
<tr>
<td>Personal computer</td>
<td>90 ms , 60 %</td>
</tr>
</tbody>
</table>

* A voltage tolerance of a ms, b% implies that the equipment can tolerate a zero voltage of a ms and a voltage of b% of nominal indefinitely.
V. CONCLUSION

In this paper, a detailed model of a Static Transfer Switch is presented. A fast voltage detection strategy and a novel transfer-gating scheme are proposed. All the conditions that influence DT and TT and, consequently, VSM and VSD experienced by the load, are described in detail. It is indicated that to evaluate STS performance, all possible combinations of pre-fault conditions, fault type and instant should be studied. For these combinations, minimum, maximum and average values of VSM and VSD need to be calculated. In the paper, measurements of three unbalanced voltage sags at the terminals of a sensitive load are used to demonstrate the performance of the proposed STS model. It is shown that the resulting VSM and VSD for these particular events, cannot generate any problems to customers’ devices, according to equipment voltage tolerance limits described at IEEE Std. 1346.

VI. REFERENCES


VII. ACKNOWLEDGMENT

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